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Universal Byte Wide Pinout: 2764 is the Key

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FOREWARD

NOTE: The following paper was presented to a recent JEDEC meeting which dealt with compatability of EPROM memory pinouts and functions.

To cover this subject in detail it was necessary to reference certain unannounced Intel products. The mention of these products should not be construed as an announcement or in any way imply product availability.

ABSTRACT

This paper describes a compatible pinout family that encompasses several classes of memory devices which fit in a standard 24 pin and 28 pin DIP site. This pinout format is equally suitable for ultraviolet erasable PROMs (EPROM), Mask ROMs, Electrically Erasable PROMs (E^2), byte wide Static RAMs, and byte wide dynamic or pseudo-static RAMs.

BACKGROUND

For several years, system designers have had available a compatible family of EPROMs from Intel that allows one kilobyte, two kilobyte or four kilobyte devices to be used interchangeably in the same socket. By anticipating the 64K (8K X 8) EPROM and using 28 pin sites, this compatible family can be extended to utilize all 28 pin devices in a single format. There are JEDEC standards which govern the pinout of the 32K EPROMs, but the approval of a dual pinout standard seems to have confused prospective users seeking family and class compatibility from the various manufacturers. These various classes of devices, which include Electrically Erasable (E^2), byte wide Static RAMs and pseudo-static RAMs, will be available from Intel and other manufacturers during 1980.

Before proceeding two key definitions of system required functions are in order:

$\overline{CE}$ (active Low Chip Enable) is located on pin 18 of the 2716, 2732 and 2732A devices. Its operation in a system is to perform the power up function in the device. The $\overline{CE}$ function is the primary control function; it is uniquely decoded from a particular pattern of system addresses. Utilizing the $\overline{CE}$ function in this manner allows all other non-selected devices in a system to be in their low power mode.

$\overline{OE}$ (active Low Ouput Enable) is located on pin 20 of the present devices. Its function in a system is to provide an independent control over the output buffers internal to the memory device, thereby allowing the READ signal from the microprocessor to be connected to all $\overline{OE}$s present in the entire memory array. In this way, the data bus is only active when required by the processor or, more exactly, when the processor requires or expects data from the memory device that was selected via the $\overline{CE}$ function.

The two control lines are ANDed inside the device; this means that only the coincident application of $\overline{CE}$ and $\overline{OE}$ will activate the output of the memory device—the application of $\overline{OE}$ alone will not cause the outputs to change from the high impedance state.

It is Intel's belief that the use of an independent output enable is the only way of assuring that there is no bus contention in a system. The use of non integrated output buffers cannot achieve the same result; they can only confine bus contention to a memory card or memory section of a large card. In addition, as processor speeds increase, greater demands are placed on memory performance—the use of external non integrated output buffers places still more requirements on the performance of the memory. In this context, the time between addresses out and data in is a fixed period of time for any given processor—all devices inserted in the path—demultiplexers, transceivers, decoders, etc., must be offset by higher performance memory speeds.

The pinout family described in this paper incorporates not only maximum flexibility for the system designer with respect to the various densities of devices that are available but also allows the freedom of flexible boundaries within the memory map for different classes of memories, after the printed circuit board and system are manufactured.

Furthermore, this pinout family maintains the system control features required for functionality as densities progress from the 32K level to the 64K level, while, if the 64K device is "squeezed" into a 24 pin package, one control pin must be given up to provide for the additional required address.

FUNCTIONALITY REQUIRED IN A UNIVERSAL PINOUT

The overall objective of Intel's compatible pinout format is to provide all of the system functions required by any memory class that may be inserted into this universal site. For this site to be truly universal, it must contain provisions for address lines that represent memory densities that have not yet been developed by semiconductor manufacturers.

The attached diagram shows the pinout of the 2764—the 8K X 8 EPROM. This is the pinout that is the key to the universal pinout. The system control pins ($\overline{CE}$ and $\overline{OE}$) have already been discussed; the address and I/O pins remain standard both with respect to TTL compatibility and physical location. There are only 5 pins that need to be discussed and defined.

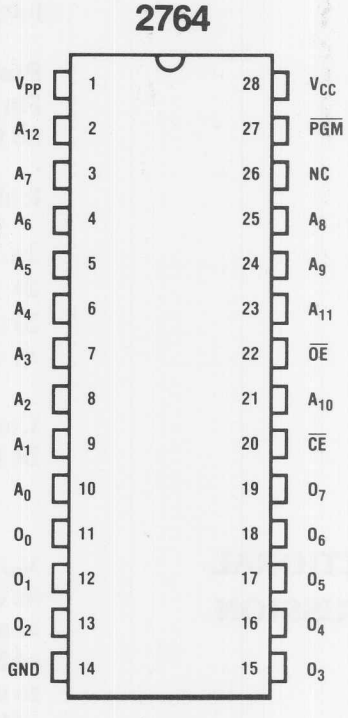


Figure 1.
The Intel 2764 (8K X 8 EPROM)
—Key to a Universal Pinout

Pin 1

Pin 1 serves as the system high voltage (V_{PP} is connected to V_{CC} for EPROM class devices). As we develop the future functionality of this pin, we will require it to serve as V_{PP} for the Write and Erase functions of the Electrically Erasable (E^2) devices, and it would also be very desirable for the 8K X 8 pseudo-static RAM to have the external refresh pin be located here—and implemented as RFSH, not $\overline{RFSH}$. (Present proposals call for $\overline{RFSH}$.) In that way, when pin 1 is tied to V_{CC}, the RAM would be self refreshing. This makes sense from a system point of view—for use with

EPROMs, this pin is tied to V_{CC} thus allowing the use of EPROMs or pseudo-static RAMs interchangeably. By busing all pin 1s together and supplying a single card edge jumper, E^2 devices could be accommodated. By implementing a jumper associated with each Pin 1, any universal site could accommodate an E^2 device, an EPROM, or a pseudo-static RAM.

Pin 2

Pin 2 is the connection for system address A_{12} for 8K X 8 and larger devices. In addition it is a control connection for the 28E2 "smart" 2K X 8 E^2 devices. As with Pin 1, a single jumper or a jumper at each site could be used to allow the use of the 28E2 in an EPROM/E^2/RAM system. The actual jumper configuration will be system dependent that is—the use of "per site" jumpers may be more efficient in some systems than a single, card edge jumper. In 28E2 board usages, per site jumpers should be provided.

Pin 28

Pin 28 is the V_{CC} supply for all devices in the universal pinout. And, because all the members of the family have a $\overline{CE}$ function, the current required by this pin will be reduced to approximately 25% of the maximum when the device is deselected.

Pin 27

Pin 27 is the writing function for all members of the universal pinout family. In the case of the EPROMs it is called $\overline{PGM}$, while for the E^2 and pseudo-static RAMs it is $\overline{WE}$. When technology advances to the point of allowing a 256K (32K X 8) EPROM, this pin will become A_{14}. This pin is effectively accommodated with a card edge jumper.

Pin 26

Pin 26 (which corresponds physically to pin 24 of a 24 pin device) is a No Connect on the 2764.

It also must serve as:

1) V_{CC} for the various devices in 24 pin packages (2716, 2732A, 21R1, etc.)
2) A_{13} for the 27E4 (16K X 8 EPROM)
3) CNTRL for the 28E2 (2K X 8 E^2)
4) CNTRL for the 21R2 (8K X 8 RAM)

Consequently, this pin may be thought of as the "class configuration pin" as it must be jumpered either at the site or at the card edge to alow total flexibility.

FUNCTIONAL DISCUSSION

V_{PP} is the signal/power supply that is required for programming of EPROMs as well as writing into E^2 devices. Since EPROMs are not normally programmed or written to in a system environment, the V_{PP} supply is set equal to V_{CC} for read only applications of EPROMs. E^2 devices require an in-system V_{PP} supply in excess of 20 volts in order to write to the device in a manner similar to EPROMs. In keeping with the tradition of locating power supplies at the corners of device sites, V_{PP} is placed on pin 1. (Although not part of the functional discussion, ground is located on pin 14 and V_{CC} is located on pin 28.) To further discuss other functions that will be present on pin 1, the refresh signal for the 8K X 8 pseudo-static RAM is placed on pin 1. As mentioned above, pin 1 will normally be tied to V_{CC} for use in EPROM systems. The active high refresh control being proposed as a standard would allow an 8K X 8 pseudo-static RAM to be inserted into the same socket and the refresh function would be taken care of automatically, that is, the pseudo-static RAM is self-refreshing with the signal RFSH tied high. (Implementation of $\overline{RFSH}$ requires an additional logic element to accomplish automatic refresh.)

The other functional control pin that needs to be discussed is write-enable ($\overline{WE}$), which is found on pin 27. This provides the write function for the pseudo-static RAM, the Static RAM, the E^2 PROM and the future class of non-volatile memory. Remembering that EPROMs are rarely programmed in a system environment; it is pin 27 that provides the $\overline{PGM}$ function for the EPROM. In a multi-memory system it is the intention that all pin 27s would be tied together and connected to the source of write-enable from the microprocessor. In a normal system WRITE pin 27 will be taken LOW; with V_{PP} at 5 volts and $\overline{CE}$ HIGH, no action will occur in an EPROM memory. To perform a write operation into an E^2 memory, V_{PP} must be greater than 20 volts, $\overline{CE}$ must be LOW and $\overline{WE}$ must be LOW. In the case where E^2 and EPROM memories are being used on the same card, and it is desired to write into the E^2, the high voltage (V_{PP}) can be supplied to all devices and only that device which received $\overline{CE}$ in proper timing with $\overline{WE}$ will be written into.

Pin 26 is a no connection on the 8K X 8 EPROM. However, it is anticipated that most system designers will connect pin 26 to V_{CC} which allows the use of 24 pin devices in the lower 24 pins of the 28 pin site. For maximum flexibility pin 26 should be jumpered on the card edge to V_{CC}.

COMPATIBILITY WITH PRESENT DEVICES

As the figure indicates, the 2732A pinout is a subset of the 28 pin universal pinout; the bottom 24 pins of the 2764 are identical to the 2732A. Likewise the 2716 is able to be inserted directly into the bottom 24 pins with the inclusion of a jumper to accommodate the V_{PP}/A_{11} changeover.

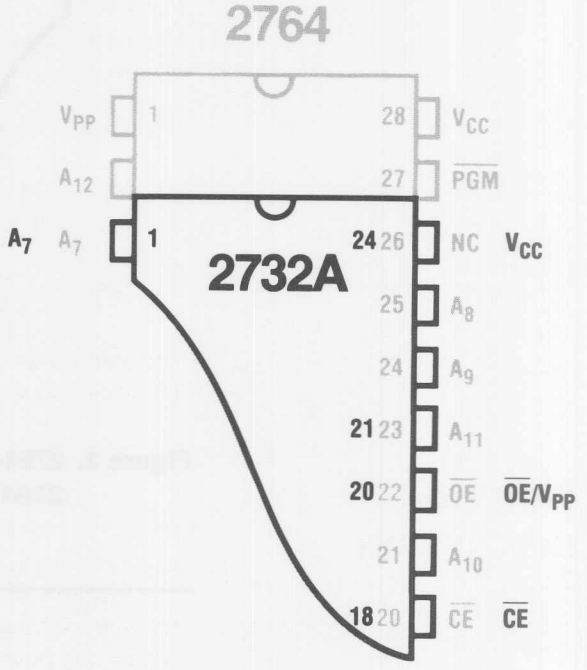


Figure 2. 2764—2732A (4K X 8 EPROM) Compatibility

In a similar manner, the 28E1 (2K X 8 E²) and the 21R1 (2K X 8 Static RAM) can be inserted in the lower 24 pins. System implementation of either of these devices require that pin 23 be appropriately jumpered—the E² device requires V_{PP} on pin 23 (pin 21 of the 24 pin device) while the RAM requires $\overline{WE}$ on that pin.

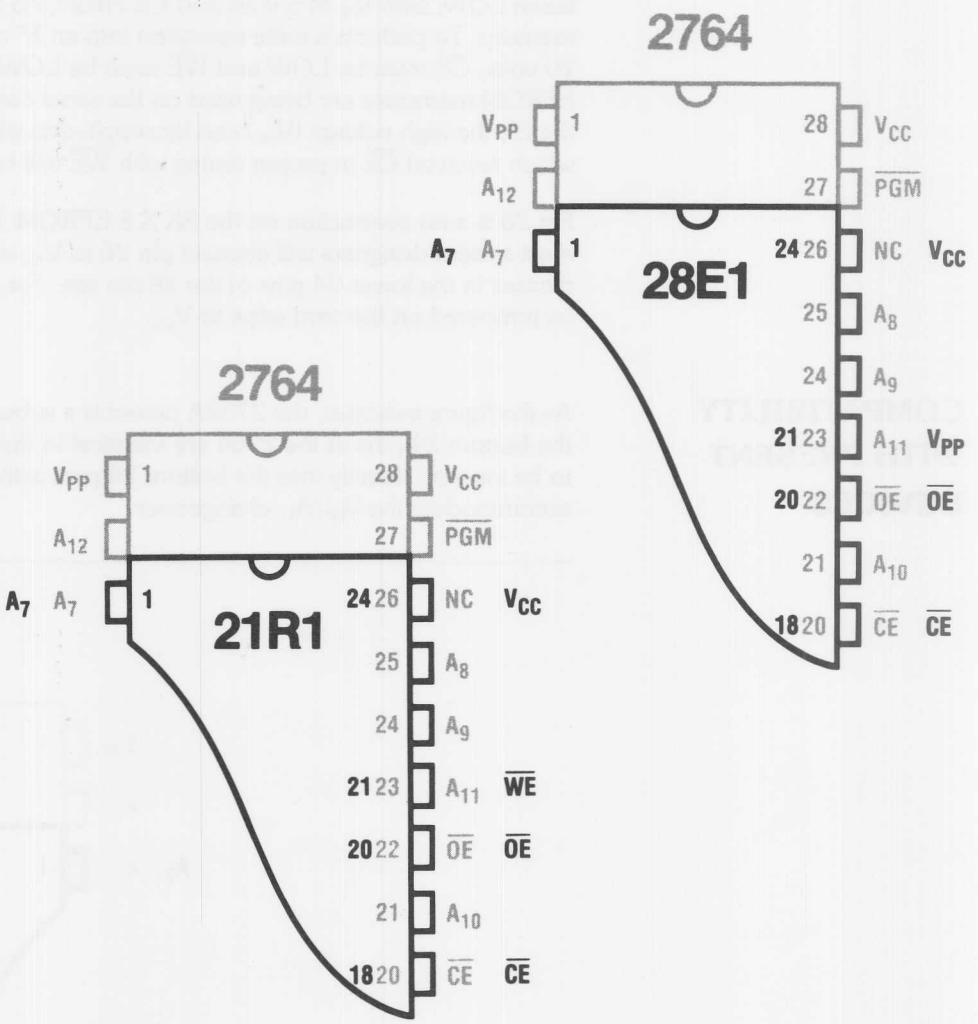


Figure 3. 2764—28E1 (2K X 8 E² PROM) and 21R1 (2K X 8 Static RAM) Compatibility

THE FUTURE

Some future devices that will fit the universal pinout are the 28E2 (2K X 8 "smart" E^2) and the 21R2 (8K X 8 pseudo-static RAM). These devices require jumpers to accommodate their functionality—in the case of the 28E2, V_{PP} must be supplied to pin 1, pins 2 and 26 require control functions. This will require a jumper for pin 2 (it is also A_{12} for 8K X 8 densities and above) while pin 26 could be hard wired if 24 pin devices are not anticipated to be used. A jumper on pin 26 will allow interchangeability with 24 pin devices, 16K X 8 EPROMs, smart 2K X 8 E^2 PROMs and 8K X 8 pseudo-static RAMs.

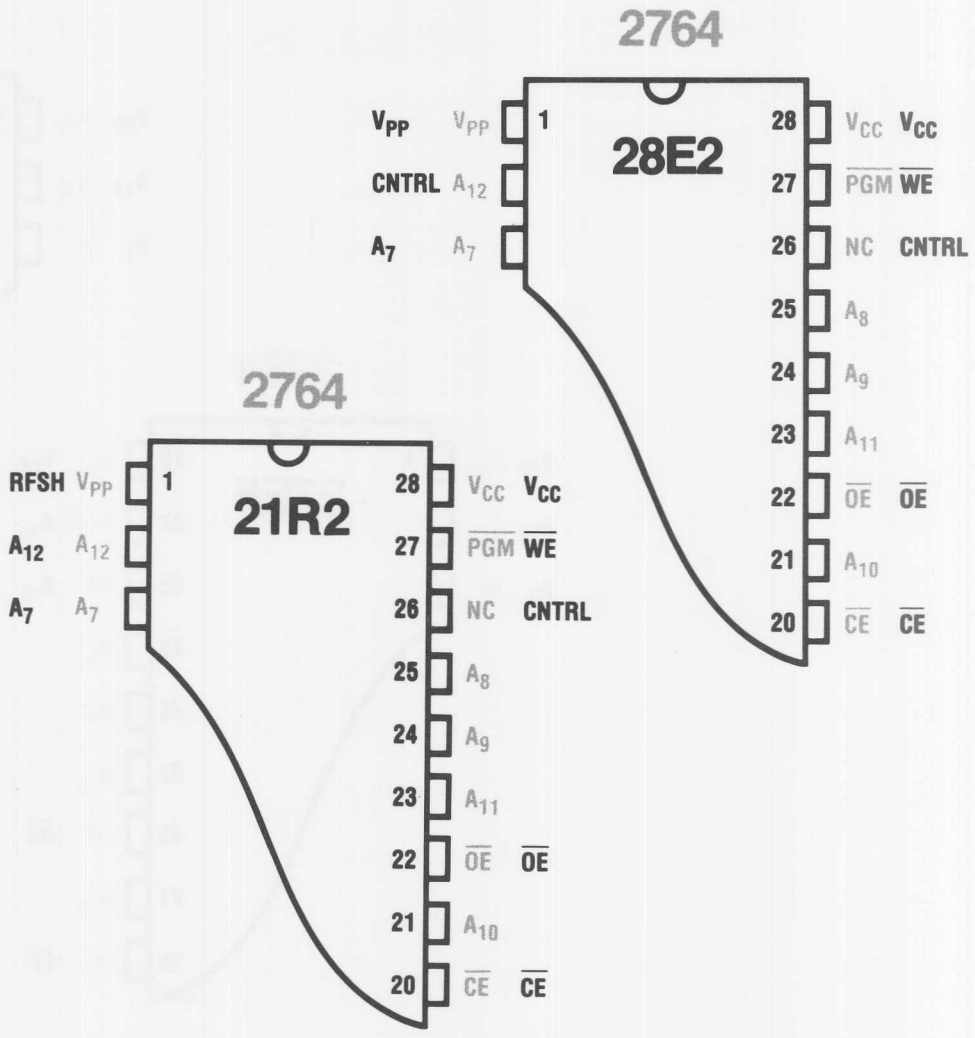


Figure 4. 2764—28E2 (2K X 8 Smart E^2 PROM) and 21R2 (8K X 8 Pseudo-Static RAM) Compatibility

State of the art technology indicates that the maximum EPROM density achievable at this point is 64 kilobits. The next technologies will provide system users with 128 K, 256 K and finally 512 kilobit devices. As these densities will be available in the early eighties, it is necessary to anticipate the total compatibility that this proposed pinout scheme provides for the user. As can be seen in the attached figure, address A_{12}, which provides the 8 kilobyte capacity, is located on pin 2 of the 2764. The most logical place for address A_{13}, which is required for a 16 kilobyte device, is on pin 26. And finally, A_{14} will appear on pin 27, the last available pin.

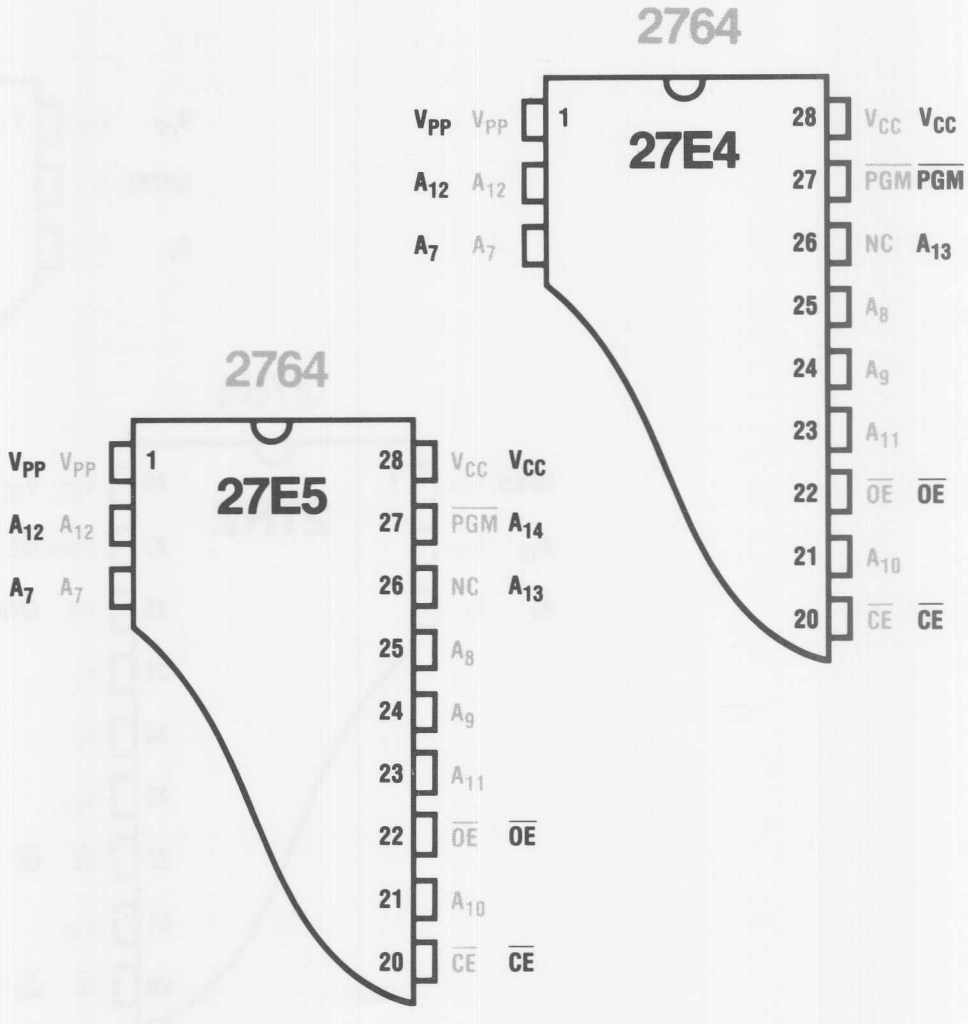


Figure 5. 2764—27E4 (16K X 8 EPROM) and 27E5 (32K X 8 EPROM) Compatibility

SUMMARY

A truly universal pinout, based on the Intel 2764 has been described in detail. It has been demonstrated that this universal pinout provides compatibility with a total of 3 classes of devices and several densities of each of the devices in a given class. The pinout accomplishes the above compatibility with an absolute minimum number of jumpers, while maintaining functional compatibility with contemporary microprocessors. And it also is compatible with Intel's plan for a future class of non volatile memories.

For purposes of comparison all required jumpers are shown in the table below. The figures which follow summarize all the pinouts of the various classes and densities discussed in this paper.

PIN 1	PIN 2	PIN 26	PIN 27
+5V	A_{12}	V_{CC}	$\overline{WE}$ ($\overline{PGM}$)
V_{PP}	CNTRL	CNTRL	A_{14}
RFSH ($\overline{RFSH}$)		A_{13}	

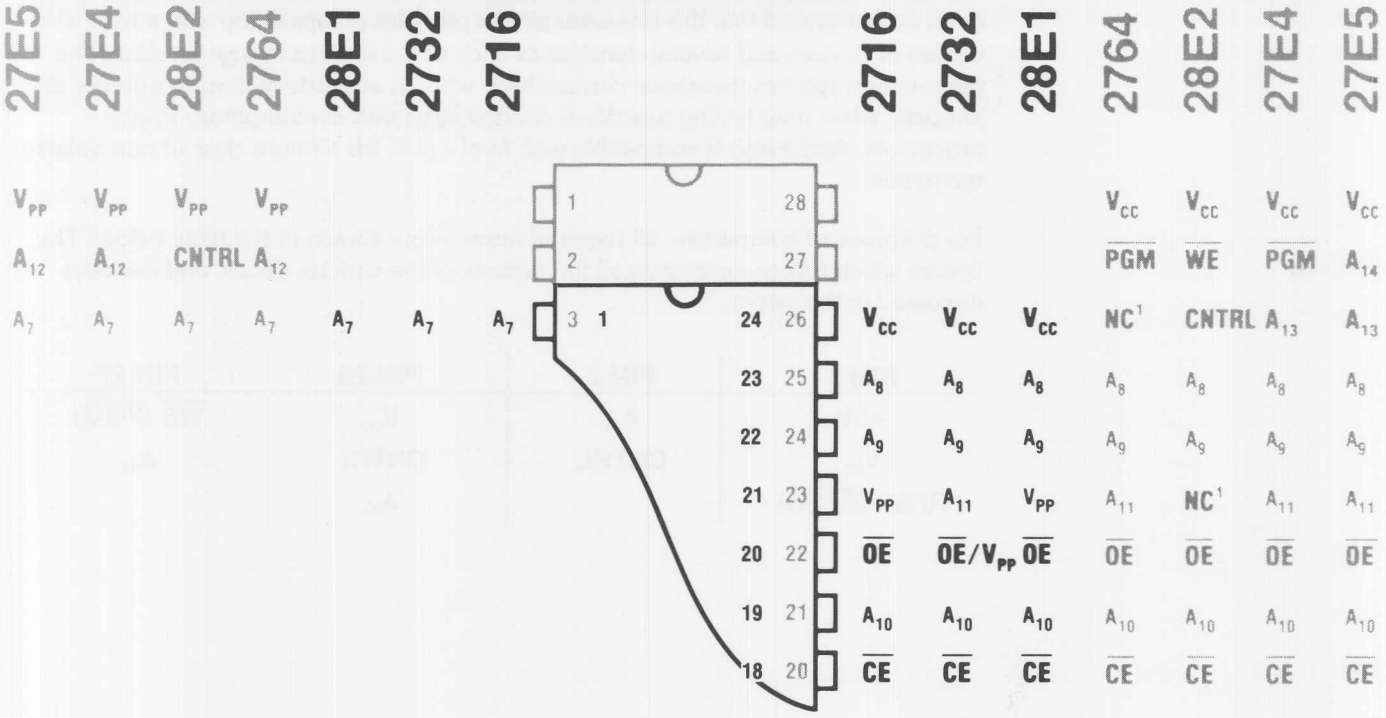
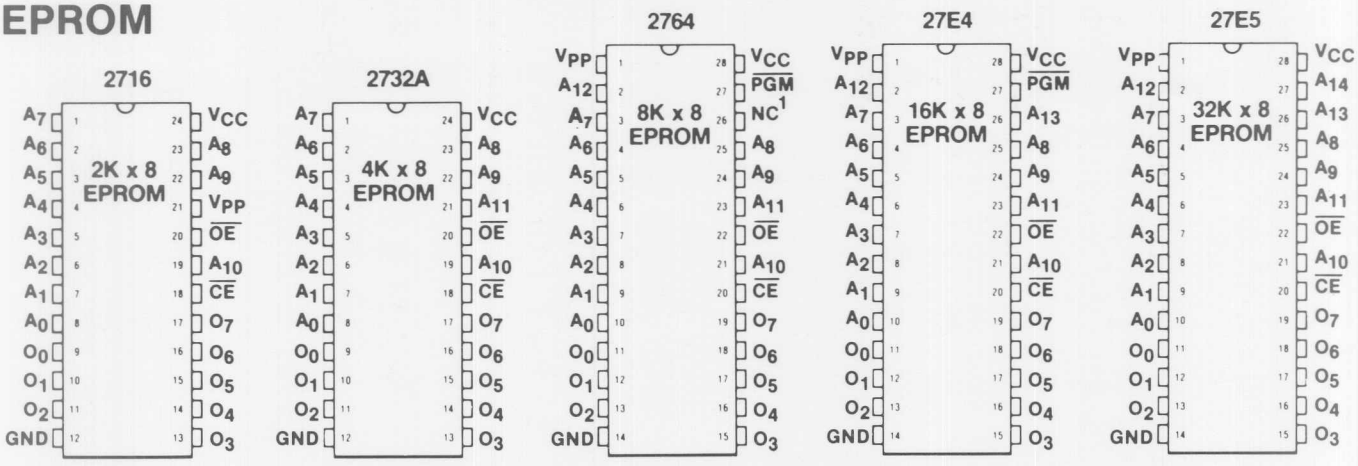


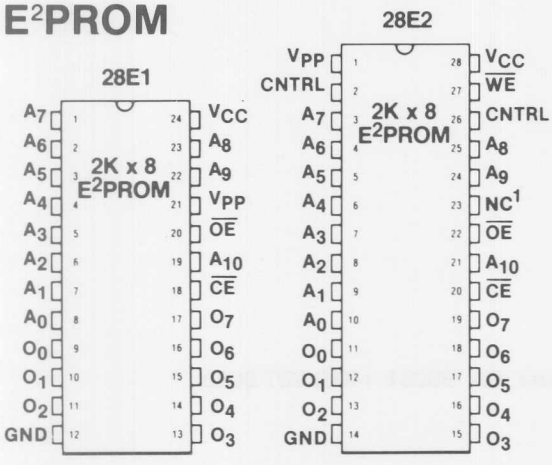
Figure 6. Pinout Summary—EPROM, E²

NOTE 1—
An address should be provided for upward compatibility.

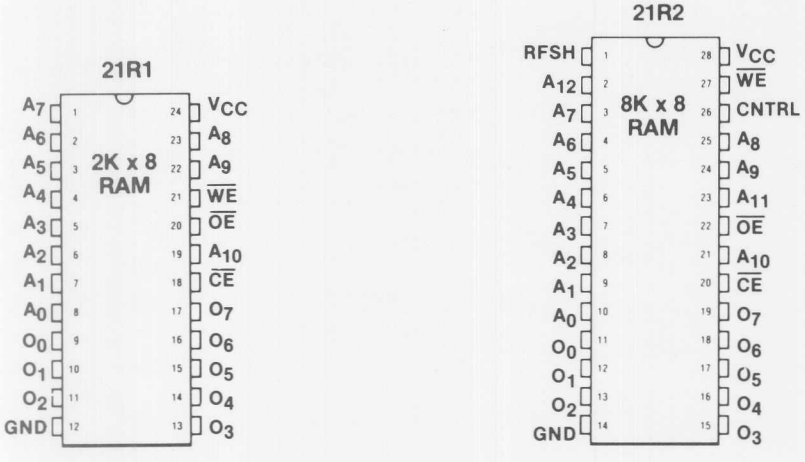
EPROM



E²PROM



RAM



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An address should be provided for upward compatibility.

Figure 7. Detailed Pinout Diagram by Class and Density

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